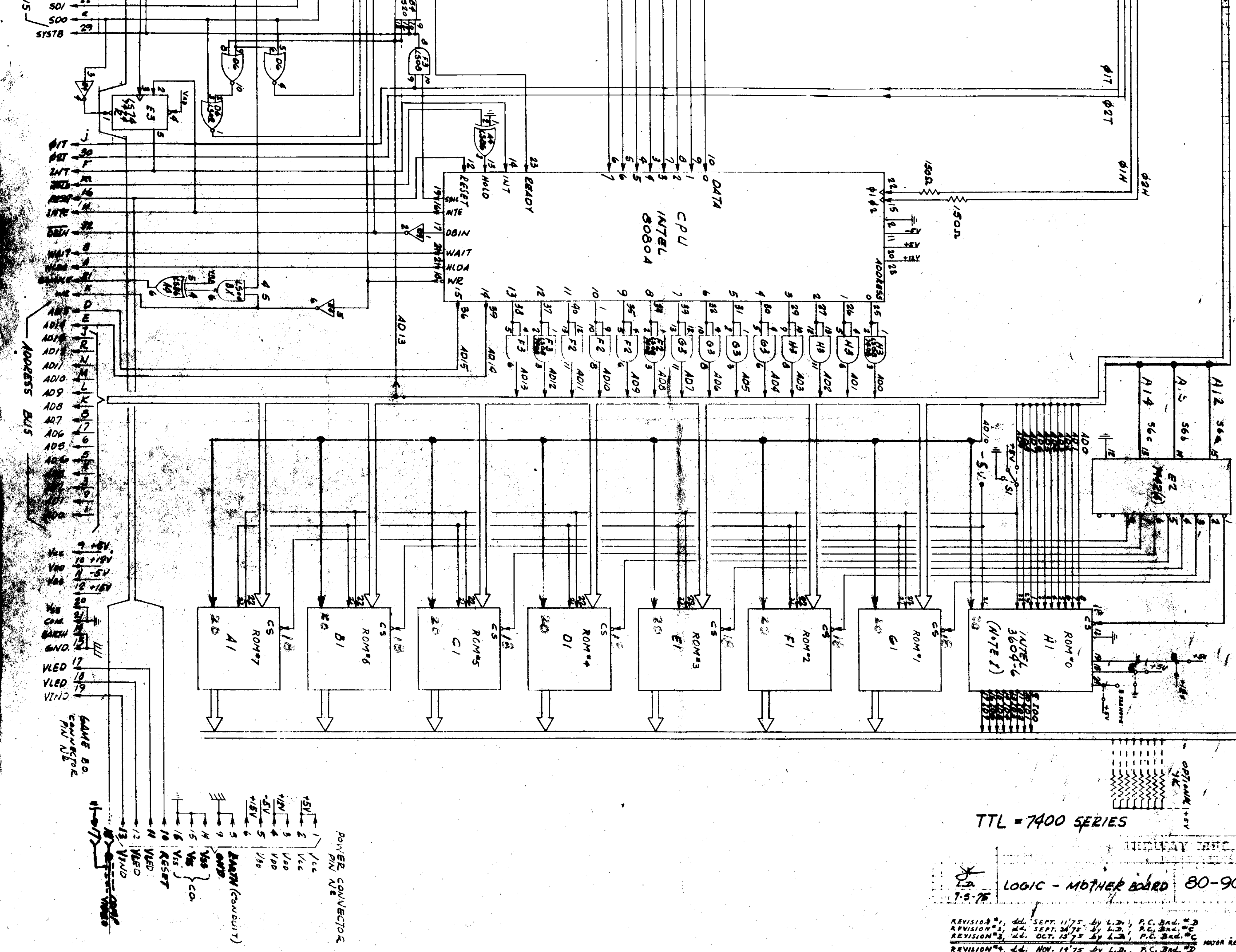
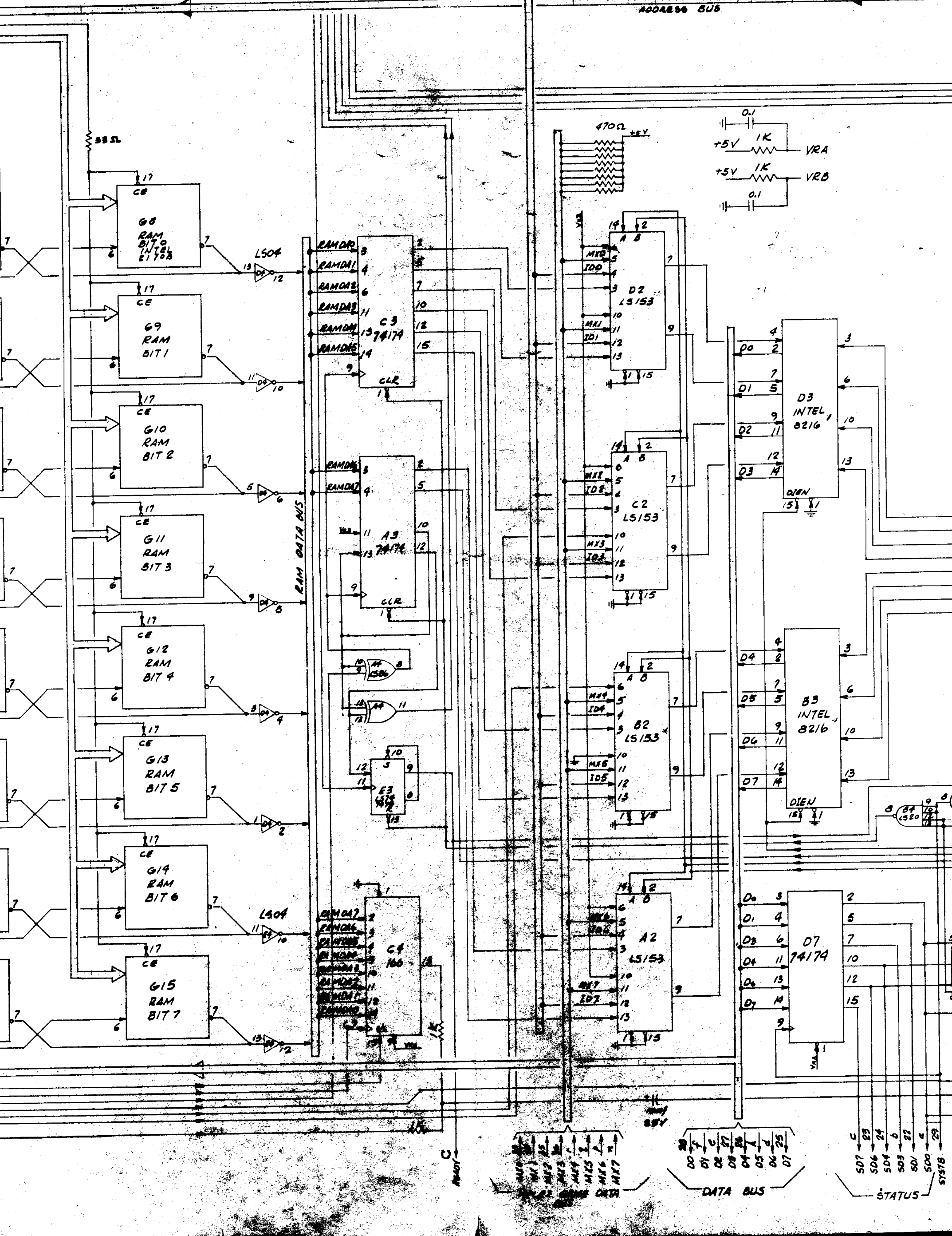
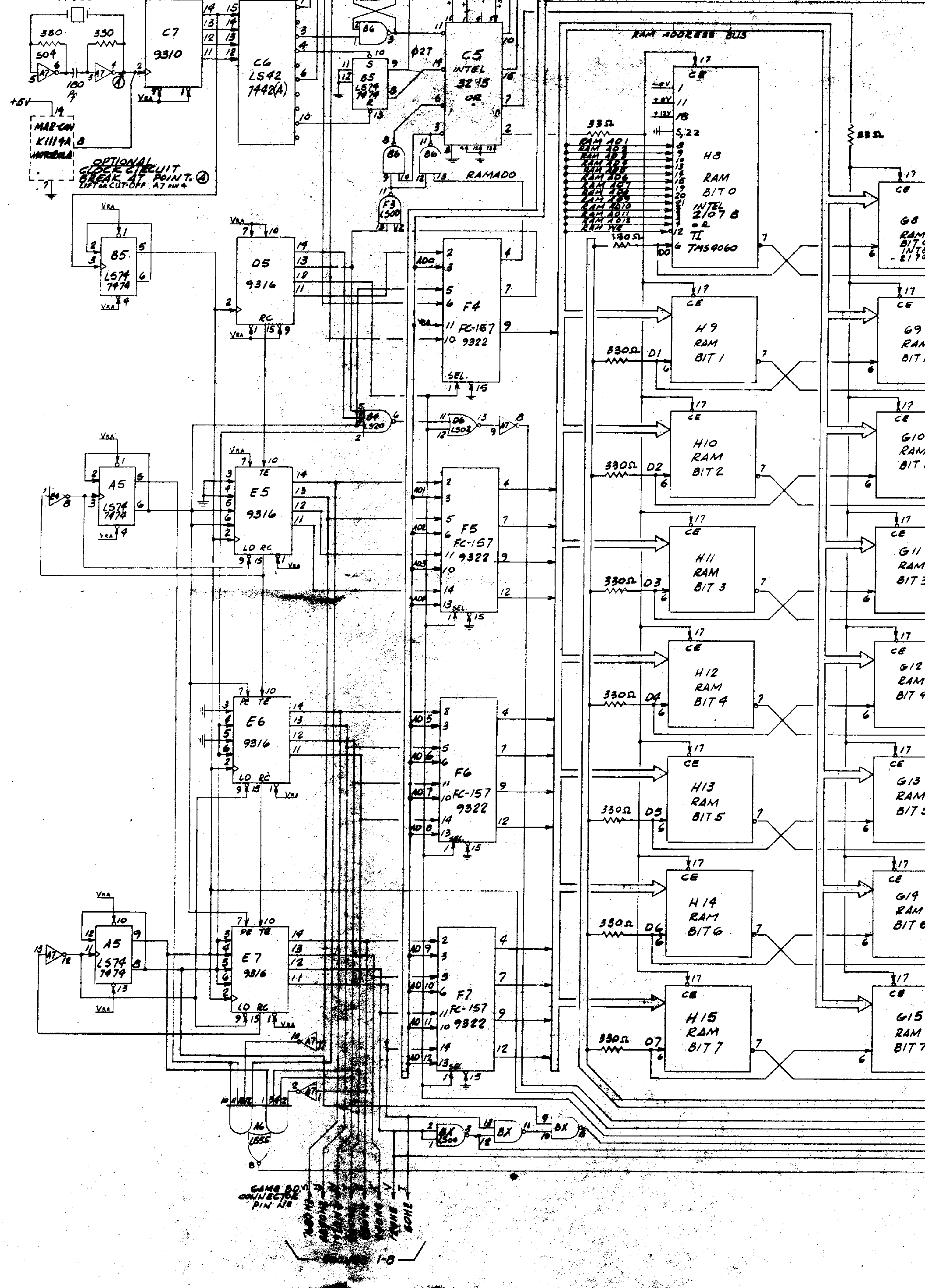
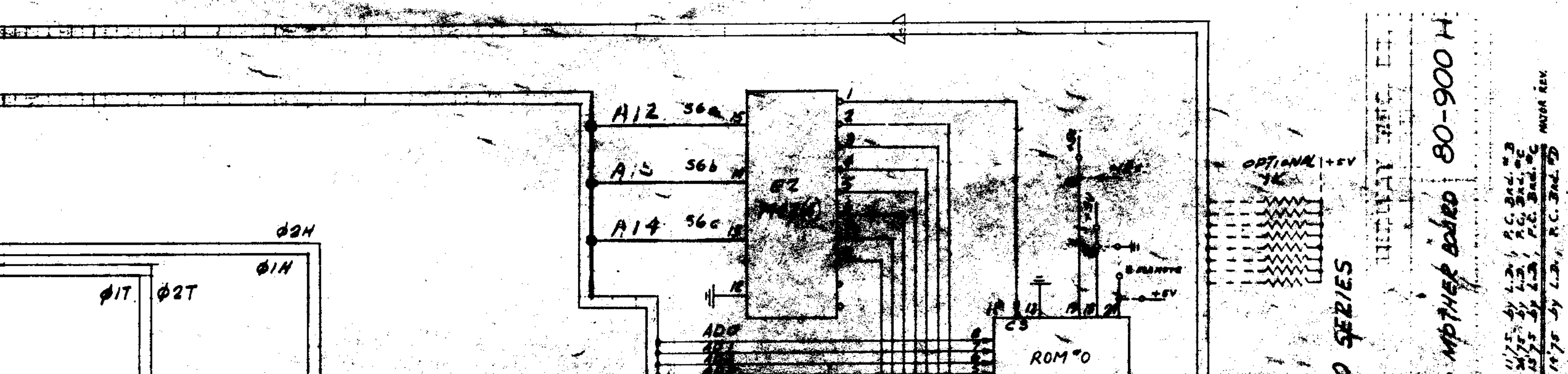


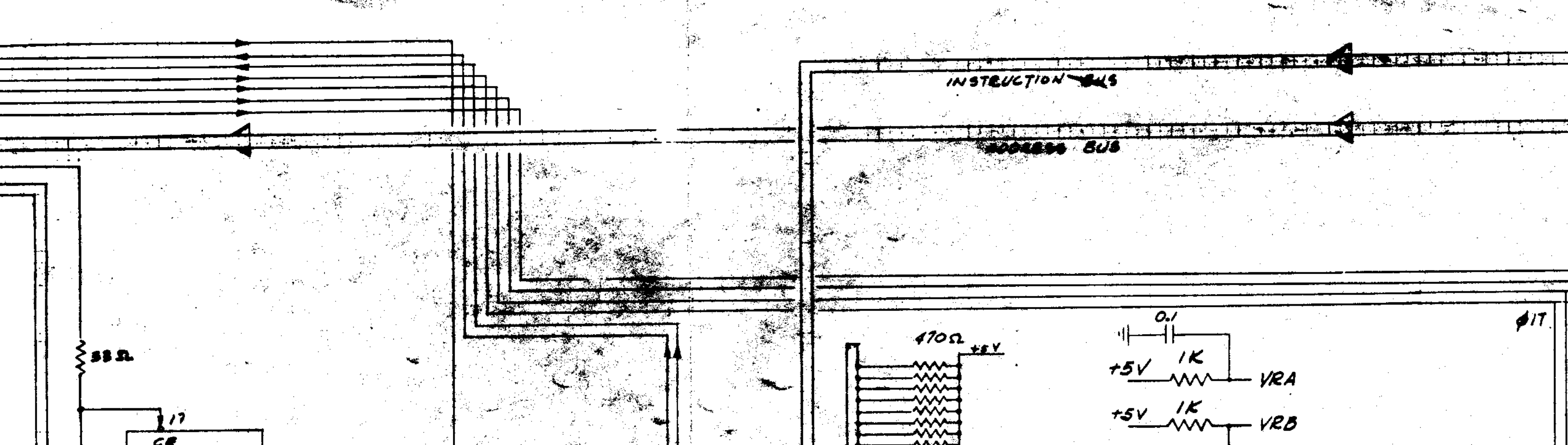
ADDRESS BUS
CPU
INTEL
8080A
DATA
ROM#7 A1
ROM#6 B1
ROM#5 C1
ROM#4 D1
ROM#3 E1
ROM#2 F1
ROM#1 G1
ROM#0 H1 INTEL 3604-6 (NOTE 1)
GAME BD. CONNECTOR PIN NE
POWER CONNECTOR PIN NE
TTL = 7400 SERIES
LOGIC - MOTHER BOARD
80-90
REVISION #1, dd. SEPT. 11'75 by L.D., P.C. Bd. #B
REVISION #2, dd. SEPT. 24'75 by L.D., P.C. Bd. #C
REVISION #3, dd. OCT. 13'75 by L.D., P.C. Bd. #C
REVISION #4, dd. NOV. 14'75 by L.D., P.C. Bd. #D
9-5-75

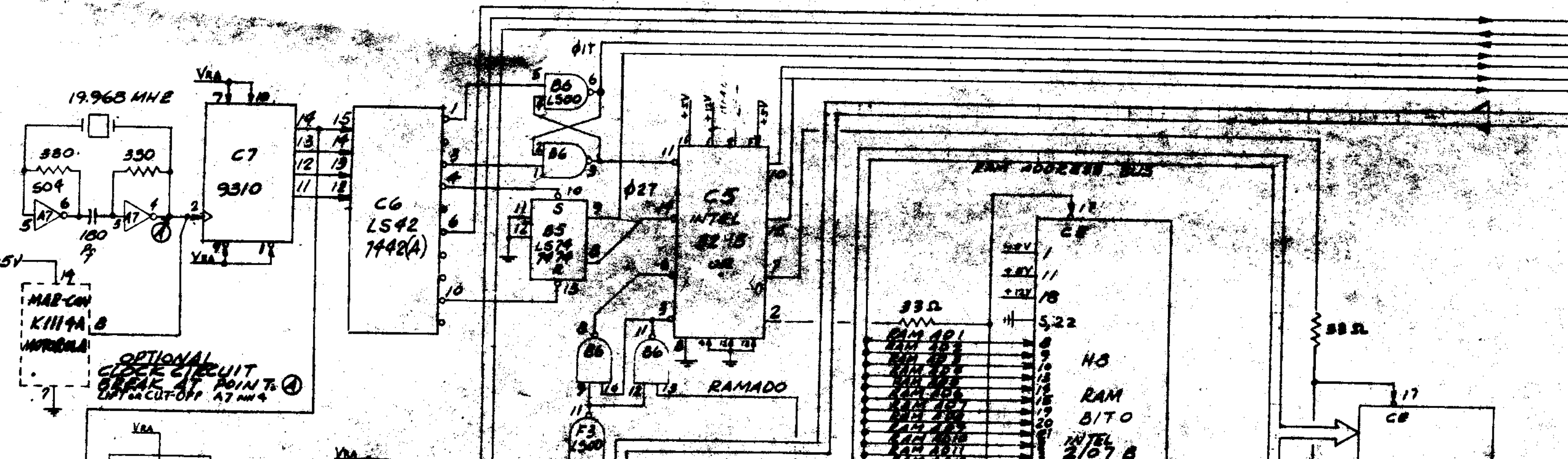

ADDRESS BUS
RAM DATA BUS
G8 RAM BIT 0 INTEL 2170B
G9 RAM BIT 1
G10 RAM BIT 2
G11 RAM BIT 3
G12 RAM BIT 4
G13 RAM BIT 5
G14 RAM BIT 6
G15 RAM BIT 7
LS04
C3 74174
A3 74174
E3 LS74
C4 166
D2 LS153
C2 LS153
B2 LS153
A2 LS153
D3 INTEL 8216
B3 INTEL 8216
D7 74174
B4 LS20
470Ω +5V
+5V 1K VRA
+5V 1K VRB
0.1
33Ω
READY
DATA BUS
STATUS
SYSTB


OPTIONAL
CLOCK CIRCUIT
BREAK AT POINT Ⓐ
LIFT or CUT-OFF A7 PIN 4
MAR-CON
K1114A
MOTOROLA
+5V
C7
9310
C6
LS42
7442(A)
B5
LS74
7474
C5
INTEL
8245
OR
Φ27
RAMADO
F3
LS00
B6
D5
9316
F4
FC-157
9322
B4
LS20
D6
LS02
A5
LS74
7474
E5
9316
F5
FC-157
9322
E6
9316
F6
FC-157
9322
E7
9316
F7
FC-157
9322
A6
LS55
BX
LS00
GAME BD'S
CONNECTOR
PIN NO
SQUARE 1-8
RAM ADDRESS BUS
H8
RAM
BIT 0
INTEL
2107 B
or
TI
TMS4060
G8
RAM
H9
RAM
BIT 1
H10
RAM
BIT 2
H11
RAM
BIT 3
H12
RAM
BIT 4
H13
RAM
BIT 5
H14
RAM
BIT 6
H15
RAM
BIT 7
G9
G10
G11
G12
G13
G14
G15
330Ω
33Ω
CE
D1
D2
D3
D4
D5
D6
D7

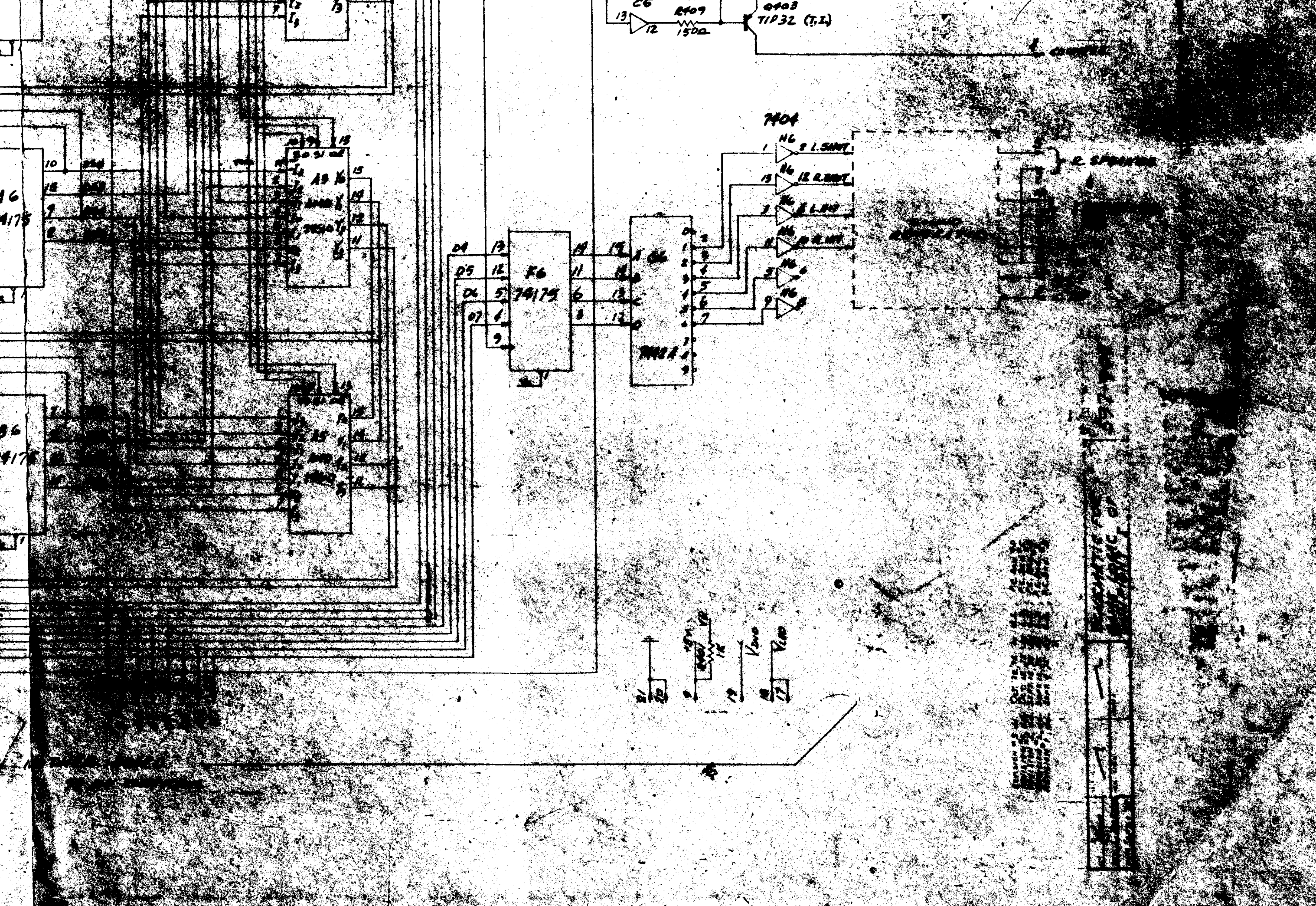


A12
56a
A13
56b
A14
56c
E2
ϕ2H
ϕ1H
ϕ1T
ϕ2T
ADO
CS
ROM #0
+5V
OPTIONAL
+5V
SERIES
MOTHER BOARD
80-900 H
MAJOR REV.

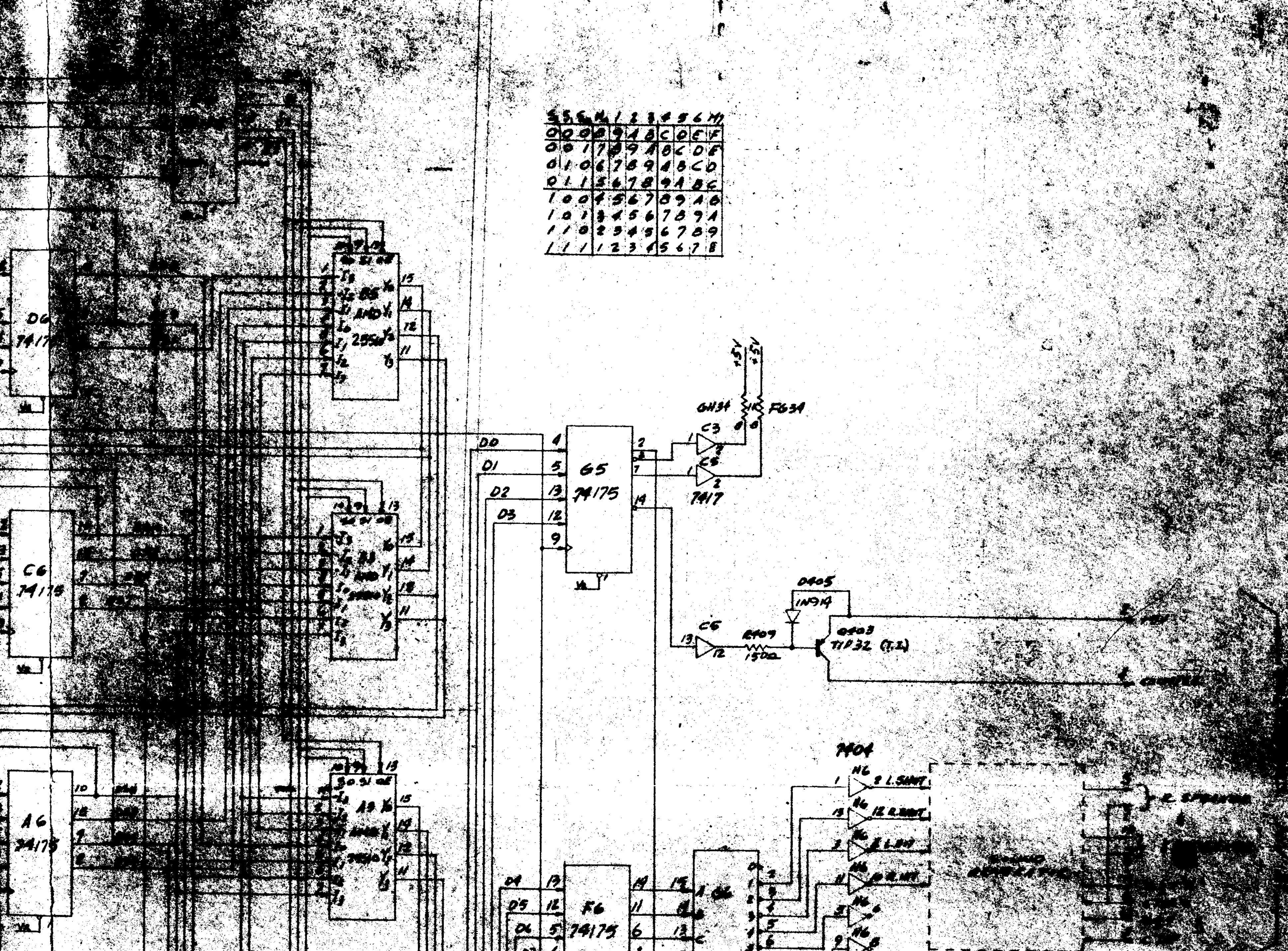

INSTRUCTION BUS
ADDRESS BUS
33Ω
17
CE
470Ω
+5V
0.1
+5V
1K
VRA
+5V
1K
VRB
ϕ17



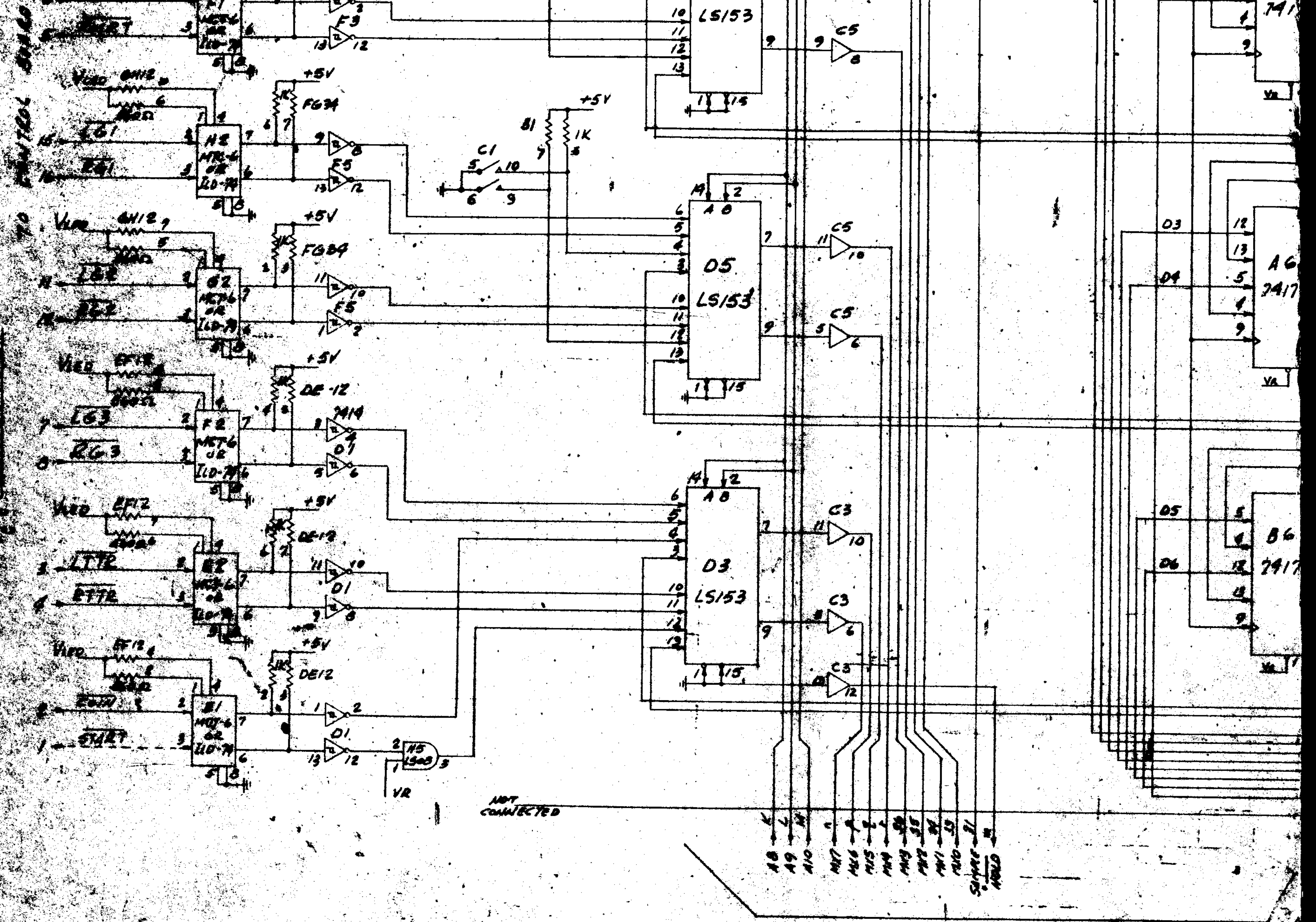
19.968 MHZ
380
330
504
A7
180
C7
9310
C6
LS42
1442(A)
B6
LS00
B5
LS74
C5
INTEL
8224
ϕ1T
ϕ2T
OPTIONAL
CLOCK CIRCUIT
BREAK AT POINT
MAB-CON
K1114A
MOTOROLA
F3
LS00
RAMADO
RAM ADDRESS BUS
33Ω
H8
RAM
BIT 0
INTEL
2107 B
CE
VRA
5V

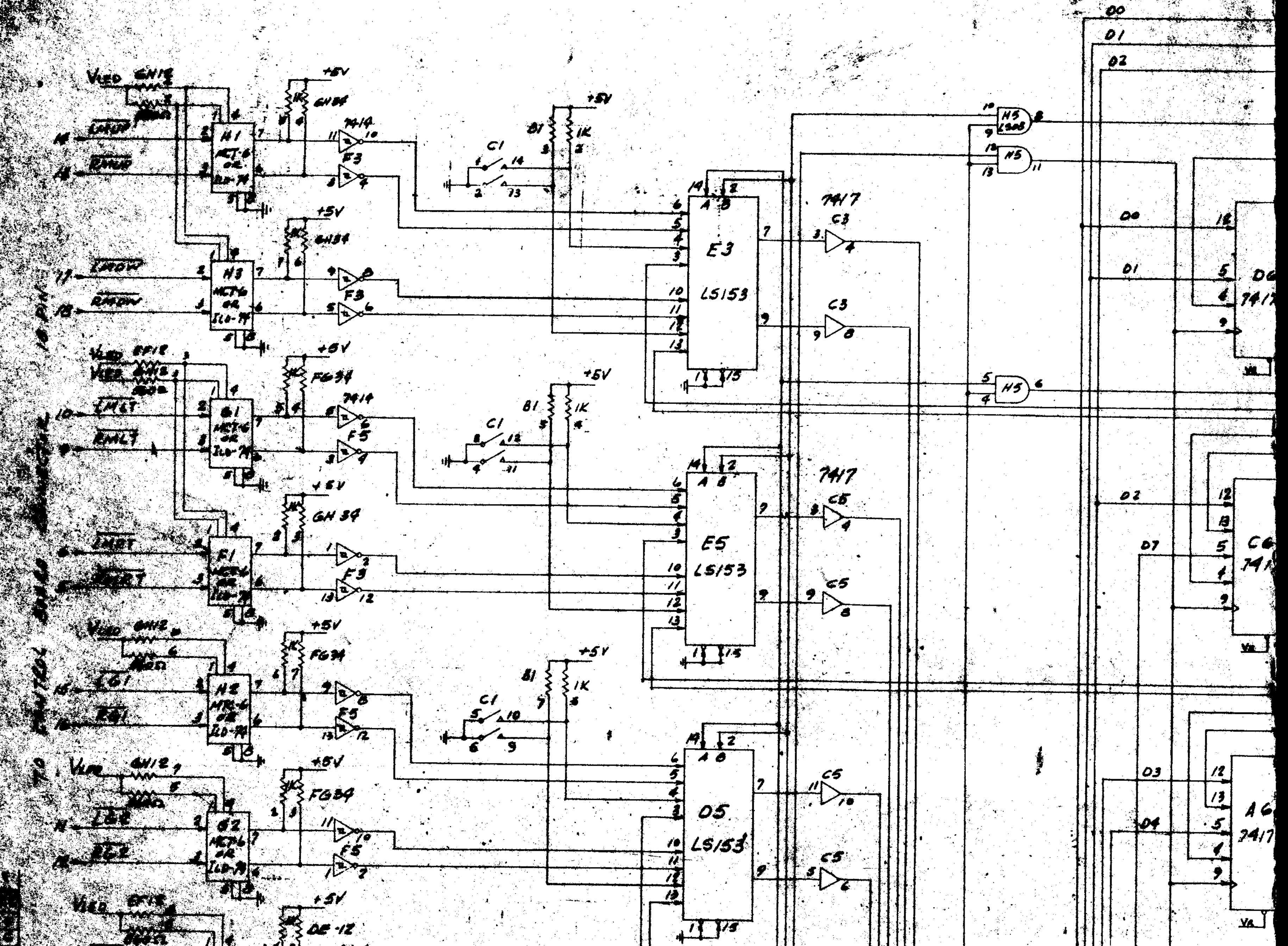


C6
R409
150Ω
Q403
TIP32 (T.I.)
7404
F6
74175
D4
D5
D6
D7

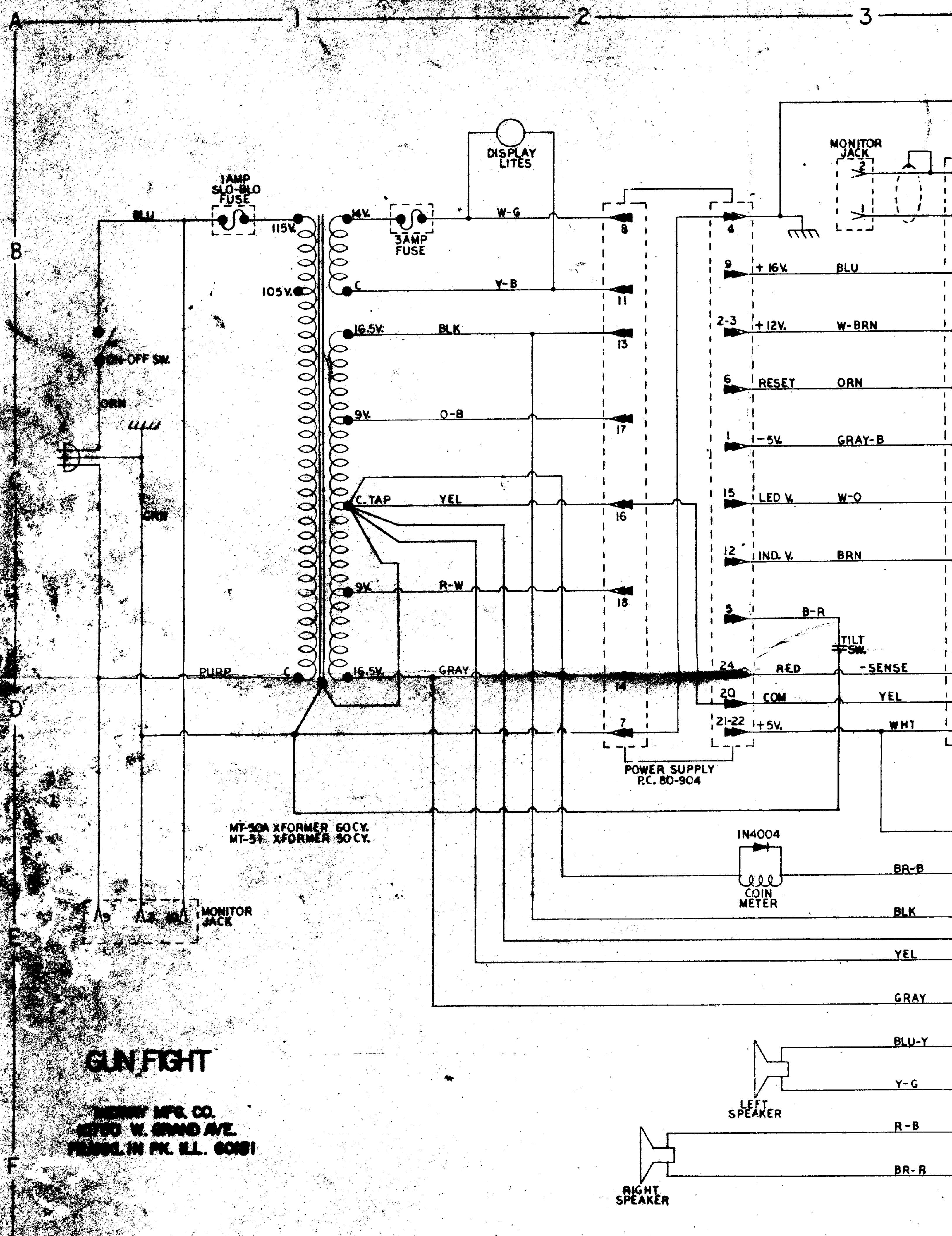


S	S	S	M	1	2	3	4	5	6	M
0	0	0	8	9	A	B	C	D	E	F
0	0	1	7	8	9	A	B	C	D	E
0	1	0	6	7	8	9	A	B	C	D
0	1	1	5	6	7	8	9	A	B	C
1	0	0	4	5	6	7	8	9	A	B
1	0	1	3	4	5	6	7	8	9	A
1	1	0	2	3	4	5	6	7	8	9
1	1	1	1	2	3	4	5	6	7	8


TO CONTROL BOARD
NOT CONNECTED
D5
LS153
D3
LS153
A8
A9
A10
SAMPLE
HOLD
+5V

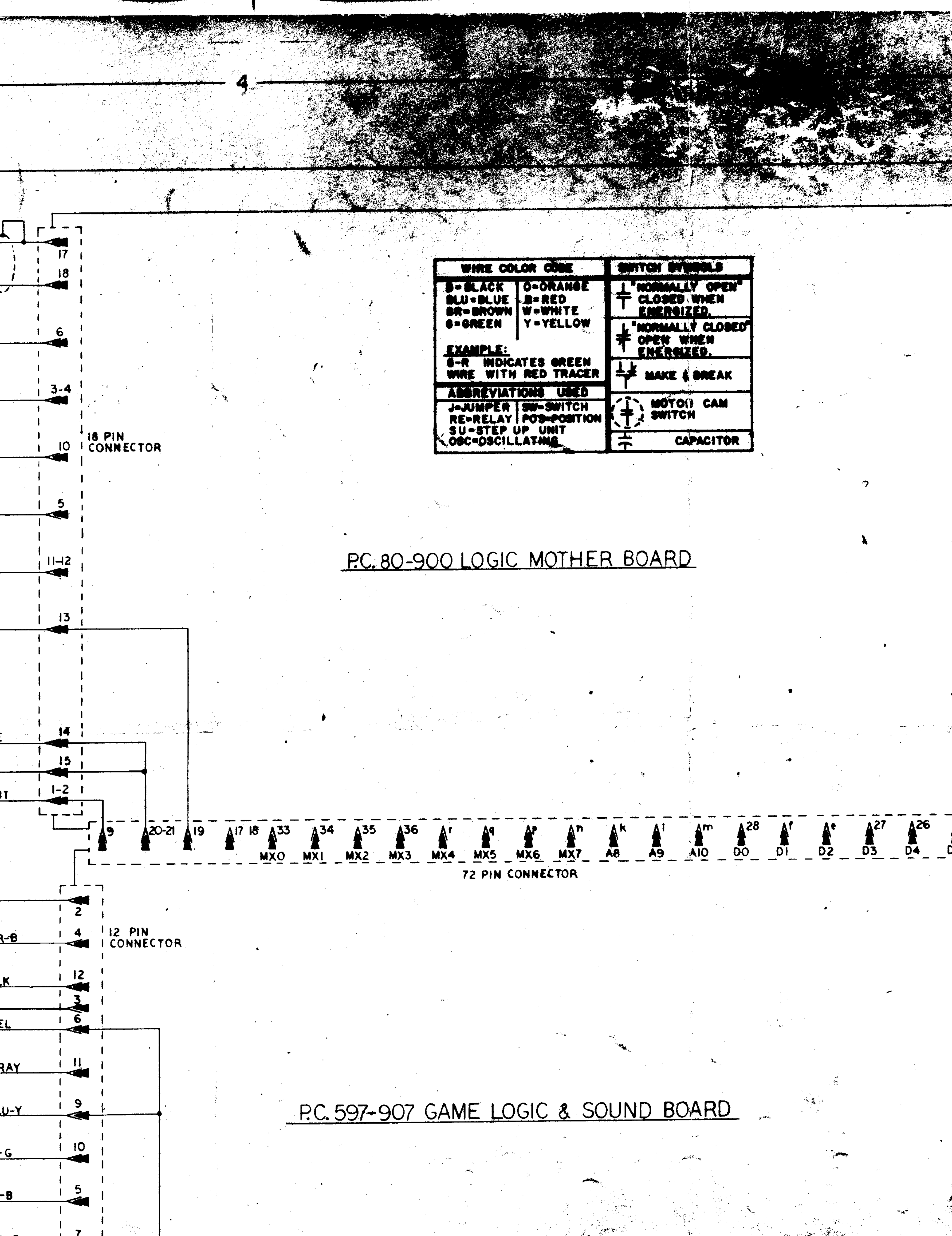


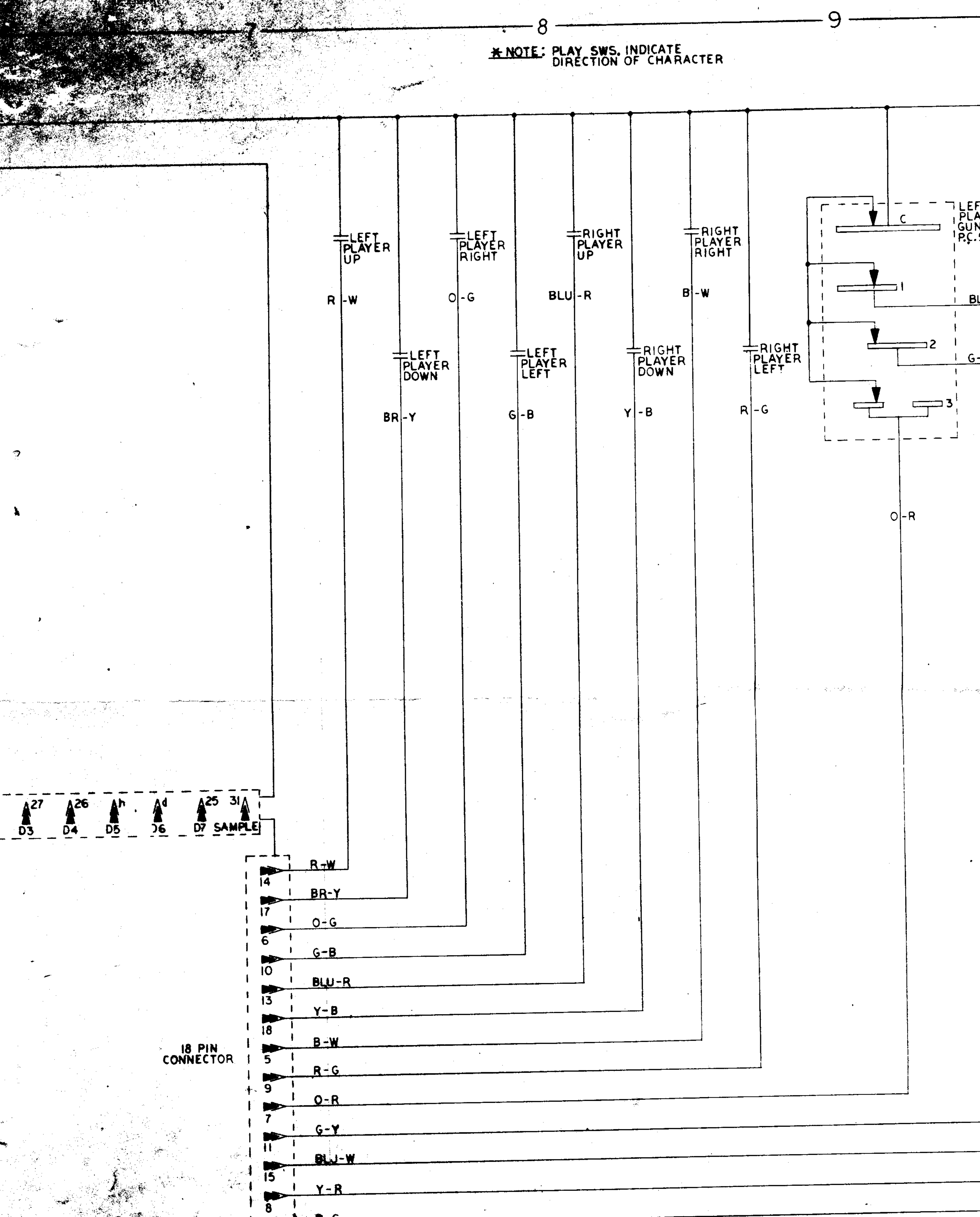
+5V
LS153
E3
E5
D5
7417
7414
H1
H3
G1
F1
H2
G2
H5
C1
B1
1K
D0
D1
D2
D3
D4
D7

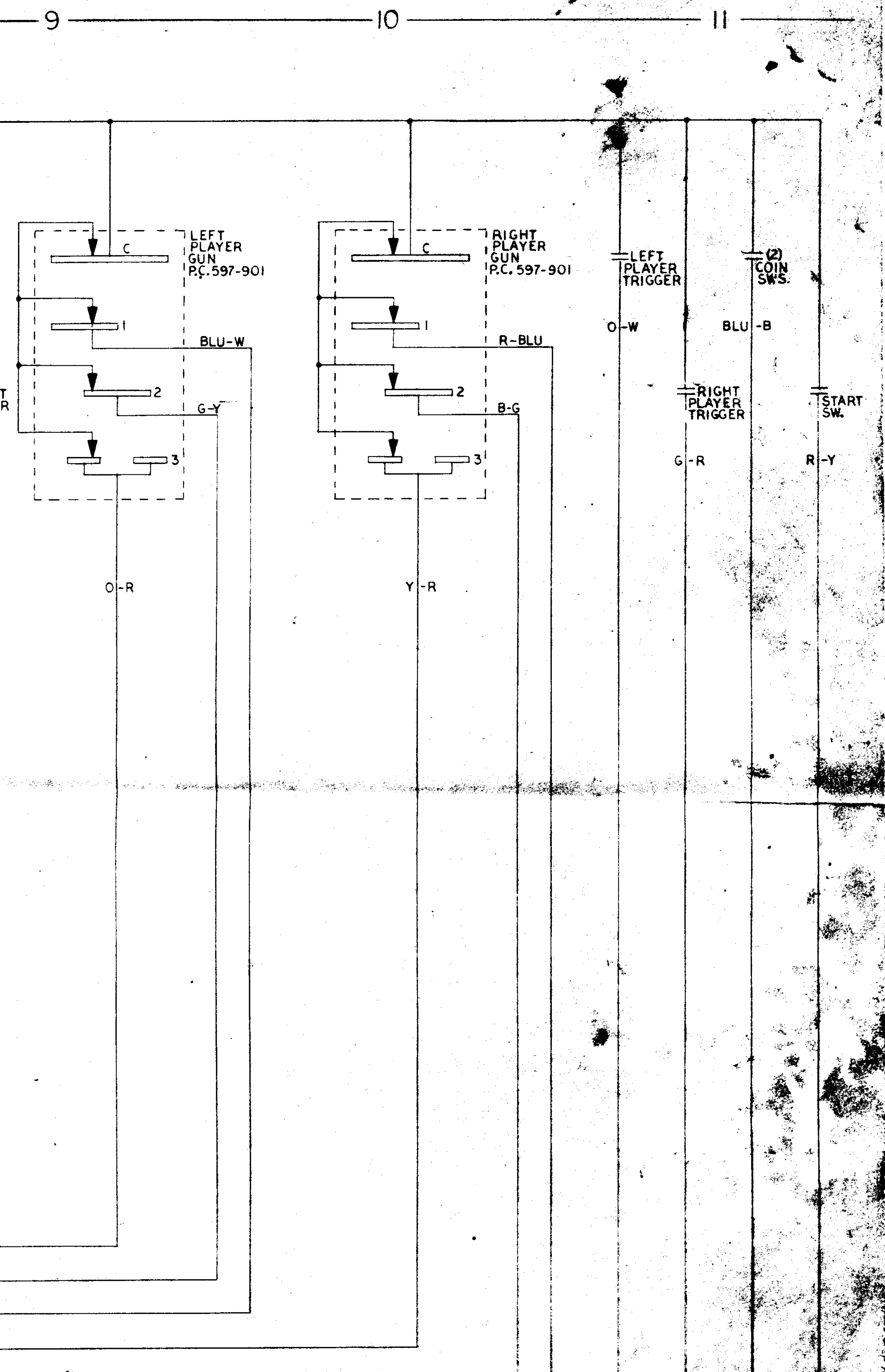


GUN FIGHT

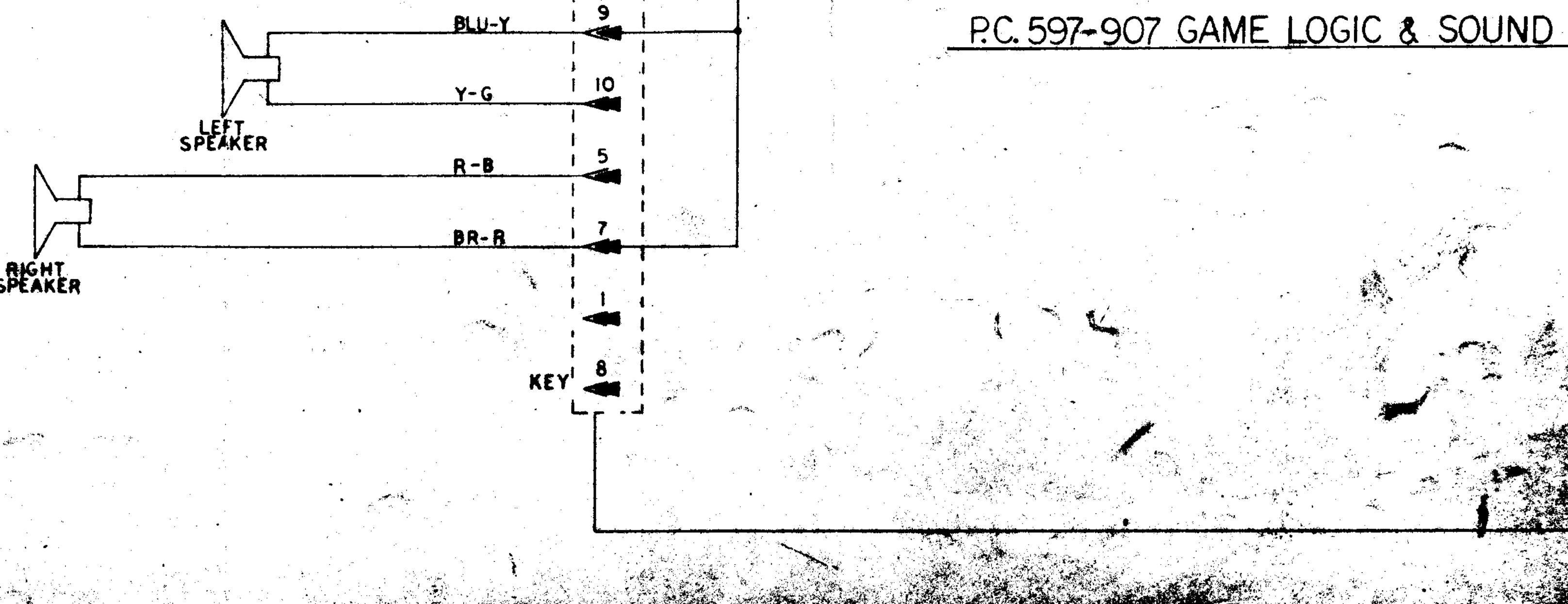
MIDWAY MFG. CO.
10750 W. GRAND AVE.
FRANKLIN PK. ILL. 60131

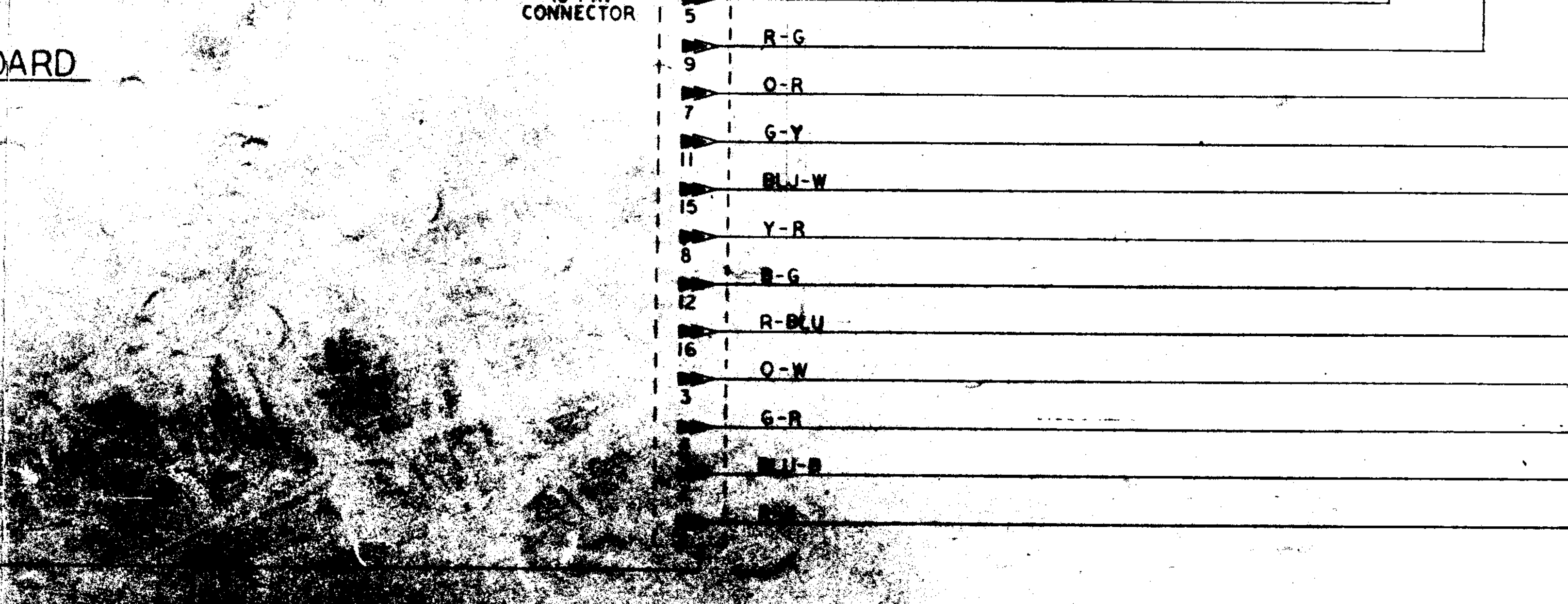

4
17
18
6
3-4
10
18 PIN CONNECTOR
5
11-12
13
14
15
1-2
9
20-21
19
17 18
33
34
35
36
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
A8
A9
A10
28
D0
D1
D2
27
D3
26
D4
72 PIN CONNECTOR
2
4
12 PIN CONNECTOR
12
3
6
11
9
10
5
7
WIRE COLOR CODE
B=BLACK
BLU=BLUE
BR=BROWN
G=GREEN
O=ORANGE
R=RED
W=WHITE
Y=YELLOW
EXAMPLE:
G-R INDICATES GREEN WIRE WITH RED TRACER
ABBREVIATIONS USED
J=JUMPER
SW=SWITCH
RE=RELAY
POS=POSITION
SU=STEP UP UNIT
OSC=OSCILLATING
SWITCH SYMBOLS
"NORMALLY OPEN" CLOSED WHEN ENERGIZED.
"NORMALLY CLOSED" OPEN WHEN ENERGIZED.
MAKE & BREAK
MOTO(?) CAM SWITCH
CAPACITOR
P.C. 80-900 LOGIC MOTHER BOARD
P.C. 597-907 GAME LOGIC & SOUND BOARD


8
9
* NOTE: PLAY SWS. INDICATE DIRECTION OF CHARACTER
LEFT PLAYER UP
LEFT PLAYER RIGHT
RIGHT PLAYER UP
RIGHT PLAYER RIGHT
R-W
O-G
BLU-R
B-W
LEFT PLAYER DOWN
LEFT PLAYER LEFT
RIGHT PLAYER DOWN
RIGHT PLAYER LEFT
BR-Y
G-B
Y-B
R-G
C
1
2
3
O-R
D3
D4
D5
D7
SAMPLE
27
26
25
31
18 PIN CONNECTOR
14
17
6
10
13
18
5
9
7
11
15
8
R-W
BR-Y
O-G
G-B
BLU-R
Y-B
B-W
R-G
O-R
G-Y
BLU-W
Y-R


9
10
11
LEFT PLAYER GUN P.C. 597-901
C
1
2
3
BLU-W
G-Y
O-R
RIGHT PLAYER GUN P.C. 597-901
R-BLU
B-G
Y-R
LEFT PLAYER TRIGGER
O-W
(2) COIN SWS.
BLU-B
RIGHT PLAYER TRIGGER
G-R
START SW.
R-Y

P.C. 597-907 GAME LOGIC & SOUND




CONNECTOR
5
R-G
9
O-R
7
G-Y
11
BLU-W
15
Y-R
8
12
R-BLU
16
O-W
3
G-R

